UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,596	12/31/2001	Howard S. David	42390.P13873	2205

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EXAMINER
LI, ZHUO H

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/039,596	DAVID, HOWARD S.
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>29 June 2006</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>9,11,12 and 16-25</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>9-11-12, 16-25</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   This Office action is in response to the amendment filed 6/29/2006.

Double Patenting

2.   The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees.   A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3.   Claims 9, 11-12 and 16-25 are rejected on the ground of nonstatutory obviousness-type

double patenting as being unpatentable over claims 1-21 of U.S. Patent No. 6,925,534. Although

the conflicting claims are not identical, they are not patentably distinct from each other because

all the claimed limitations in the current application are transparent found in U.S. Patent No.

6,925,534 with obvious wording variations. The following table shows the example of taking

claim 16 of current application compared with claims 1, 4 and 7 of U.S. Patent No. 6,925,534.

Application 10/039,596	U.S. Patent No. 6,925,534
16. A memory controller, comprising:	1. An apparatus, comprising:
an array of tag address storage locations; and	An array of tag address storage locations; and
a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory module of a system memory, the command sequencer and serializer to deliver a writeback command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the memory module.	a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module via a plurality of command lines over an interconnect, the command sequencer and serializer unit to cause a current line of data to be read out from a first location of a memory module memory device and to load a next line of data from a second location of the memory module memory device to the data cache, in response to a single command having a plurality of segments serialized and sequentially transmitted via the plurality of address lines and command lines over the interconnect

	within a single memory transaction, wherein the single command includes at least one of memory module destination information, cache way information, address strobe state information, cache hit information, column address information, and memory device bank information, wherein the single command is delivered over a plurality of transfer periods within a single memory access transaction, and wherein the cache hit information is transferred during a last transfer period of the transfer periods.
	4. The apparatus of claim 1, wherein each of the segments is transmitted within one of the transfer periods over one of the command and address lines.
	7. The apparatus of claim 1, wherein a segment of the command transmitted in the last transfer period of a command line includes eviction information of an eviction buffer of the data cache.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5.   Claim 23 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US PAT.

6,477,621 hereinafter Lee).

Regarding claim 23, Lee discloses a system memory (1009, figure 5) comprising at least

two memory modules (300a through 300n, figure 5), each memory modules including at least

one memory device (301-304, figure 3) and a data cache (601, figure 3) coupled to an eviction

buffer (701, figure 3), both coupled to the memory device (col. 8 lines 7-42).

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 20-22 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Lee et al. (US PAT. 6,477,621 hereinafter Lee) in view of Akkary et al. (US PAT. 5,526,510

hereinafter Akkary).

Regarding claim 20, Lee discloses a memory module (300, figure 3) comprising at least

one memory device (301-304, figure 3) and a data cache (601, figure 3) coupled to an eviction

buffer (701, figure 3), both coupled to the memory device (col. 8 lines 7-42), the data cache

controlled by a plurality of commands, i.e., read or write command, delivered by an external

memory master, i.e., a memory controller, over a bus, i.e., a memory system interface (314,

figure 3 and col. 9 line 48 through col. 10 line 20). Lee differs from the claimed invention in not

specifically teaching the memory module to receive a write back command, the write back

command to cause a previous line of data, evicted from the data cache and stored within the

eviction buffer, to be written out of the eviction buffer to the memory device. However, Akkary

teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write

back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2)

to perform memory operation in responds to an instruction from a central processing unit,

wherein the write back buffer is capable of temporary storing the eviction entry from the cache

bank, and further write back to a main memory such that a pervious line of data evicted from the

data cache, which stored within the write back buffer, is written out of the write back buffer to

the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to modify Lee in having the

memory module to receive a write back command, the write back command to cause a previous

line of data, evicted from the data cache and stored within the eviction buffer, to be written out of

the eviction buffer to the memory device, as per teaching of Akkary, because it avoids coherency

problems and performs replace operation more quicker.

Regarding claim 21, Akkary teaches the data cache to evict previous line of adapt the

data cache into the eviction buffer according to an eviction signal received from the memory

controller (col. 6 lines 12-20 and col. 6 line 34 through col. 8 line 27).

Regarding claims 24-25, Lee differs from the claimed invention in not specifically

teaching a memory module to receive a write back command, the write back command to cause a

previous line of data, evicted from the data cache and stored within the eviction buffer, to be

written out of the eviction buffer to the memory device of the memory module and wherein the

memory stores a current line of data within the data cache of the memory module. However,

Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and

a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308,

figure 2) to perform memory operation in responds to an instruction from a central processing

unit, wherein the write back buffer is capable of temporary storing the eviction entry from the

cache bank, and further write back to a main memory such that a pervious line of data evicted

from the data cache, which stored within the write back buffer, is written out of the write back

buffer to the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been

obvious to a person of ordinary skill in the art at the time the invention was made to modify Lee

in having the memory module to receive a write back command, the write back command to

cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to

be written out of the eviction buffer to the memory device of the memory module and wherein

the memory stores a current line of data within the data cache of the memory module, as per

teaching of Akkary, because it avoids coherency problems and performs replace operation more quicker.

8.   Claims 9, 11-12 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,378,049 hereinafter Stracovsky) in view of Lee et al. (US PAT. 6,477,621 hereinafter Lee) and Akkary et al. (US PAT. 5,526,510 hereinafter Akkary).

Regarding claim 9, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller (104, figure 1B) coupled to the processor, the memory controller including an array of tag address storage locations (114, figure 1B) and a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage locations, and a system memory (108, figure 1B) coupled to the memory controller (col. 6 lines 17-45). Stracovsky differs from the claimed invention in not specifically teaching the system memory including at least two memory modules, each memory module including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device, and the data cache controlled by a plurality of commands delivered by the memory controller. However, Lee teaches a system memory (1009, figure 5) comprising at least two memory modules (300a through 300n, figure 5), each memory modules including at least one memory device (301-304, figure 3) and a data cache (601, figure 3) coupled to an eviction buffer (701, figure 3), both coupled to the memory device (col. 8 lines 7-42), and the data cache controlled by a plurality of commands, i.e., read or write command, delivered by an external memory master, i.e., a memory controller, over a bus, i.e., a memory system interface (314, figure 3 and col. 9 line 48 through col. 10 line 20) in order to flexibly serve different memory

masters as required by data processing system to which the memory system is connected (col. 3

lines 24-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the

time the invention was made to modify Stracovsky in having the system memory including at

least two memory modules, each memory module including at least one memory device and a

data cache coupled to an eviction buffer, both coupled to the memory device, and the data cache

controlled by a plurality of commands delivered by the memory controller, as per teaching of

Lee, because it flexibly serves different memory masters as required by data processing system

to which the memory system is connected. Furthermore, neither Stracovsky nor Lee specifically

discloses the memory controller writing a current line of data to the data cache and the memory

controller to further instruct the data cache to evict a previous cache line of data cache into the

eviction buffer. However, Akkary teaches in a data cache system comprising a plurality of cache

banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory

via a system bus (308, figure 2) to perform memory operation in responds to an instruction from

a central processing unit, wherein the write back buffer is capable of temporary storing the

eviction entry from the cache bank, and further write back to a main memory such that a

pervious line of data evicted from the data cache, which stored within the write back buffer, is

written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to modify the combination of Stracovsky and Lee in having the memory

controller writing a current line of data to the data cache and the memory controller to further

instruct the data cache to evict a previous cache line of data cache into the eviction buffer, as per

teaching of Akkary, because it avoids coherency problems and performs replace operation more

quicker.

Regarding claim 11, Akkary discloses the memory controller to deliver a writeback

command to the data cache, the writeback command to cause the previous line of data to be

written out of the eviction buffer to the memory device (col. 6 lines 12-20 and col. 6 lines 34

through col. 8 line 27).

Regarding claim 12, Akkary discloses the writeback command including way

information and bank address information (col. 7 line 48 through col. 8 line 16).

Regarding claim 16, Stracovsky discloses a memory controller (104, figure 1B)

comprising an array of tag address storage locations (114, figure 1B) and a command sequencer

and serializer unit (116, figure 1B) coupled to the array of tag address storage location, the

command sequencer and serializer unit to control the system memory (col. 6 lines 17-45).

Stracovsky differs from the claimed invention in not specifically teaching a data cache and an

eviction buffer located on at least one memory module of the system memory. However, Lee

teaches a data cache (601, figure 3) and an eviction buffer (701, figure 3) located on at least one

memory module (300a through 300n, figure 5) of a system memory (1009, figure 5) in order to

flexibly serve different memory masters as required by data processing system to which the

memory system is connected (col. 3 lines 24-35). Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to modify Stracovsky in

having the data cache and the eviction buffer located on at least one memory module of the

system memory, as per teaching of Lee, because it flexibly serves different memory masters as

required by data processing system to which the memory system is connected. Furthermore,

neither Stracovsky nor Lee specifically discloses the command sequencer and serializer unit to

deliver a writeback command to the eviction buffer associated with memory module, the write

back command to cause a previous line of data evicted from the data cache and stored within the

eviction buffer, to be written out to the memory device of the memory module. However, Akkary

teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write

back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2)

to perform memory operation in responds to an instruction from a central processing unit,

wherein the write back buffer is capable of temporary storing the eviction entry from the cache

bank, and further write back to a main memory such that a pervious line of data evicted from the

data cache, which stored within the write back buffer, is written out of the write back buffer to

the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to modify the combination

of Stracovsky and Lee in having the command sequencer and serializer unit to deliver a

writeback command to the eviction buffer associated with memory module, the write back

command to cause a previous line of data evicted from the data cache and stored within the

eviction buffer, to be written out to the memory device of the memory module, as per teaching of

Akkary, because it avoids coherency problems and performs replace operation more quicker.

Regarding claims 17-18, Akkary discloses the memory controller issuing an eviction

signal to the data cache to evict the previous line of data from the data cache into the eviction

buffer, and also issuing the writeback command cause the previous line of data to be written out

of the eviction buffer to the memory device once the memory device is idle (col. 6 lines 12-20

and col. 6 lines 34 through col. 8 line 27).

Regarding claim 19, Akkary teaches a processor to cause a current line of data to be written from the processor (318, figure 2) to the data cache (318, figure 2) via fill buffer (320, figure 2), the processor to cause the previous line of data to be evict out of the data cache to the eviction buffer, i.e., writeback buffer (322, figure 2 and col. 6 line 12 through col. 8 line 27).

Response to Arguments

9.   Applicant's arguments with respect to claims 9, 11-12 and 16-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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